16-Bit, 4-Channel, 250 kSPS PulSAR® ADC

Preliminary Technical Data

AD7682

FEATURES

- 16-bit resolution with no missing codes
- 4-channel multiplexer with:
  - Unipolar single ended or
  - Differential (GND sense)/pseudo-bipolar inputs
- Throughput: 250 kSPS
- INL/DNL: ±0.6 LSB typical
- Dynamic range: 93.5 dB
- SINAD: 92.5 dB @ 20 kHz
- THD: –100 dB @ 20 kHz
- Analog input range:
  - 0 V to V_{REF} with V_{REF} up to VDD
- Reference:
  - Internal selectable 2.5 V/4.096 V or
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor
- Channel sequencer, selectable 1-pole filter, BUSY indicator
- No pipeline delay, SAR architecture
- Single-supply 2.7V – 5.5 V operation with 1.8 V to 5 V logic interface
- Serial interface SPI®/QSPI™/MICROWIRE™/DSP compatible
- Power dissipation:
  - 6 mW @ 5 V/100 kSPS
- Standby current: 1 nA
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Battery-powered equipment
  - Medical instruments
  - Mobile communications
  - Personal digital assitants
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process Control

FUNCTIONAL BLOCK DIAGRAM

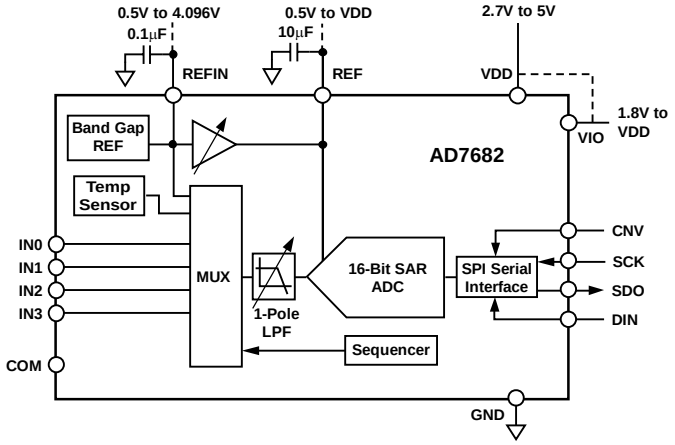

Figure 1.

Table 1. Multichannel14-/16-Bit PulSAR ADC

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-x
16-Bit	4	AD7682		ADA4841-x
16-Bit	8	AD7689	AD7699	ADA4841-x

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GENERAL DESCRIPTION

The AD7682 is a 4-channel 16-bit, charge redistribution successive approximation register (SAR), analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7682 contains all of the components for use in a multi-channel, low power, data acquisition system including: a true 16-bit SAR ADC with no missing codes; a 4-channel, low crosstalk multiplexer useful for configuring the inputs as single ended (with or without ground sense), differential or bipolar; an internal low drift reference (selectable 2.5V or 4.096V) and buffer; a temperature sensor; a selectable 1-pole filter; and a sequencer useful when channels are continuously scanned in order.

The AD7682 uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level.

Power dissipation scales with throughput.

The AD7682 is housed in a tiny 20-lead LFCSP with operation specified from –40°C to +85°C.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
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SPECIFICATIONS

VDD = 2.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar mode	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	
Analog Input CMRR	f_{IN} = 250 kHz		TBD		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance					
THROUGHPUT					
Conversion Rate	VDD = 4.096V to 5.5	0		250	kSPS
	VDD = 2.5V to 4.096V	1		200	
Transient Response	Full-scale step			1.8	µs
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		-2	±0.6	+2	LSB[1]
Differential Linearity Error		−1	±0.25	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.5		LSB
Gain Error[2]		−30	±0.5	+30	LSB
Gain Error Match			TBD		LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error[2]		−5	±0.5	+5	LSB
Offset Error Match			TBD		LSB
Offset Error Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1		ppm
AC ACCURACY[3]					
Dynamic Range			93.5		dB[4]
Signal-to-Noise	f_{IN} = 20 kHz, VREF = 5V		92.5		dB
	f_{IN} = 20 kHz, VREF = 2.5V		88.5		
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, VREF = 5V		92.5		dB
	f_{IN} = 20 kHz, VREF = 2.5V		88.5		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		110		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		-117		dB
Intermodulation Distortion[5]			115		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Selectable	0.425	1.7		MHz
Aperture Delay	VDD = 5V		2.5		ns

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[1] LSB means least significant bit. With the 5 V input range, one LSB is 76.3 µV.
[2] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[3] With V_{REF} = 5 V, unless otherwise noted.
[4] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[5] f_{IN1} = 21.4 kHz and f_{IN2} = 18.9 kHz, with each tone at −7 dB below full scale.

VDD = 2.5 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
Output Voltage	For 4.096 V output, @ 25°C	4.086	4.096	4.106	V
	For 2.5 V output, @ 25°C	2.490	2.500	2.510	V
Temperature Drift	−40°C to +85°C		±TBD		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±TBD		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C_{REF} = 22 µF		TBD		ms
EXTERNAL REFERENCE					
Voltage Range	REF Input	0.5		VDD + 0.3	V
	REFIN Input (Buffered)	0.5		VDD − 0.2	V
Current Drain	250 kSPS, REF = 5V		50		µA
TEMPERATURE SENSOR					
Output Voltage[1]	@ 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[2]					
Pipeline Delay[3]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[4, 5]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5V , 100 kSPS throughput		6		mW
	VDD = 5V , 250 kSPS throughput		15		mW
	VDD = 5V , 250 kSPS throughput internal reference and buffer enabled		18.5		mW
Energy per Conversion			50		nJ
TEMPERATURE RANGE[6]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

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[1] The output voltage is internal and present on a dedicated multiplexer input.
[2] Unipolar mode: serial 16-bit straight binary
Bipolar mode: serial 16-bit 2's complement.
[3] Conversion results available immediately after completed conversion.
[4] With all digital inputs forced to VIO or GND as required.
[5] During acquisition phase.
[6] Contact an Analog Devices sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = **4.5 V to 5.5 V**, VIO = 2.3 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. [1]

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4			µs
CNV Pulse Width	t_{CNVH}	10			ns
Data Write/Read During Conversion	t_{DATA}			1.5	µs
SCK Period	t_{SCK}	15			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			25	ns
CNV Low to SCK High	t_{CLSCK}	10			ns
DIN Valid Setup Time	t_{SDIN}	4			ns
DIN Valid Hold Time	t_{HDIN}	4			ns

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[1] See Figure 2 and Figure 3 for load conditions.

VDD = **2.5 V to 4.5 V**, VIO = 2.3 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5. [1]

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
CNV Pulse Width	t_{CNVH}	10			ns
Data Write/Read During Conversion	t_{DATA}			0.7	µs
SCK Period	t_{SCK}	25			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				35	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			25	ns
CNV Low to SCK High	t_{CSCK}	10			ns
SDI Valid Setup Time	t_{SDIN}	5			ns
SDI Valid Hold Time	t_{HDIN}	4			ns

[1] See Figure 2 and Figure 3 for load conditions.

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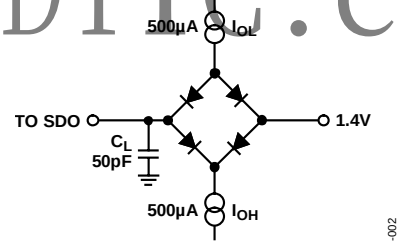

Figure 2. Load Circuit for Digital Interface Timing

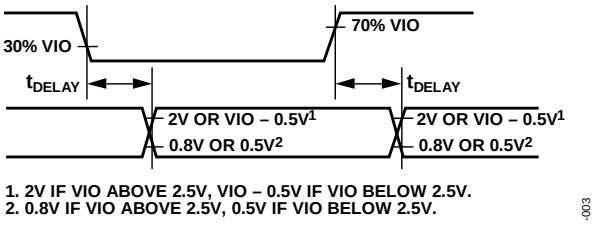

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
INn, COM	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
DIN, CNV, SCK to GND	−0.3 V to VIO + 0.3 V
SDO to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MSOP-10)	200°C/W
θ_{JC} Thermal Impedance (MSOP-10)	44°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

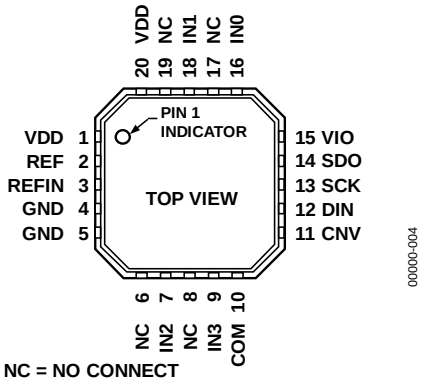

Figure 4. 20-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference, and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for 2.5V output, the minimum should be 2.7V. When using the internal reference for 4.096V output, the minimum should be 4.5V.
2	REF	AI/O	Reference Input/Output. When the internal reference is enabled, this pin produces a selectable system reference = 2.5V or 4.096V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096V max.) useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5V to VDD). For any reference method, this pin needs decoupling with an external a 10 µF capacitor connected as close to REF as possible. See
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1µF capacitor. When using the internal reference buffer, apply a source between 0.5V to 4.096V which is buffered to the REF pin as described above.
4, 5	GND	P	Power Supply Ground.
7, 9, 16, 18	IN2, IN3, IN0, IN1	AI	Analog Inputs.
10	COM	AI	Common Channel Input. All channels [7:0] can be referenced to a common mode point of 0 V or V_{REF}/2 V.
11	CNV	DI	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the BUSY indictor is enabled.
12	DIN	DI	Data Input. This input is used for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on ADO and clock in data on DIN in an MSB first fashion.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

[1]AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

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TYPICAL PERFORMANCE CHARACTERISTICS

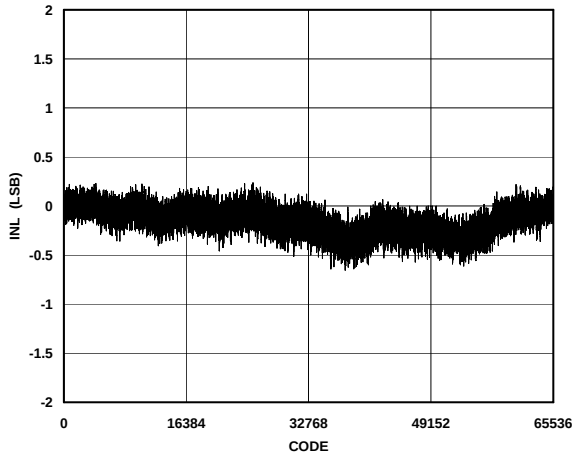

Figure 5. Integral Nonlinearity vs. Code, VREF = 5V

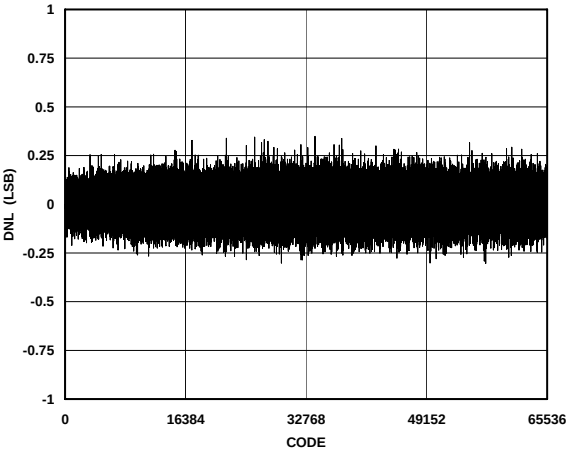

Figure 8. Differential Nonlinearity vs. Code, VREF = 5V

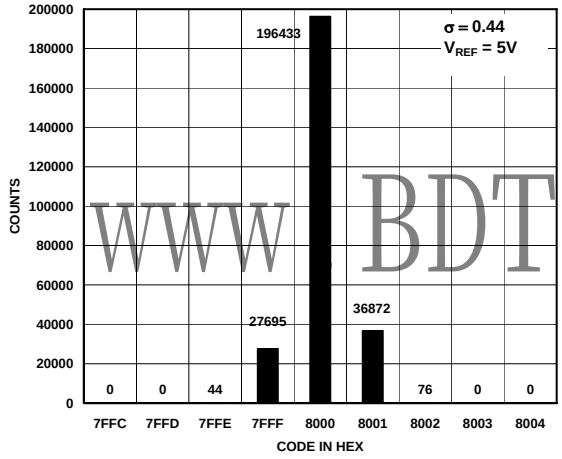

Figure 6. Histogram of a DC Input at Code Center, VREF = 5V

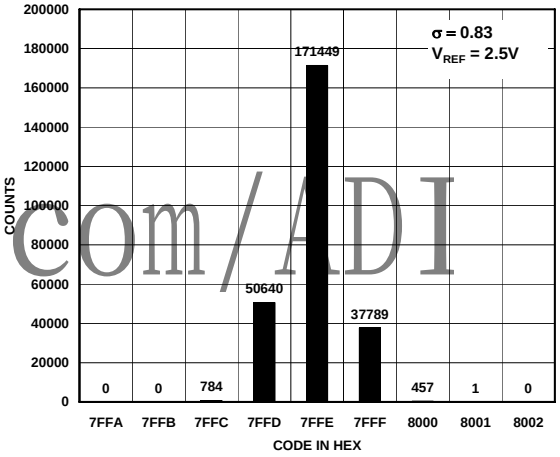

Figure 9. Histogram of a DC Input at Code Center, VREF = 2.5V

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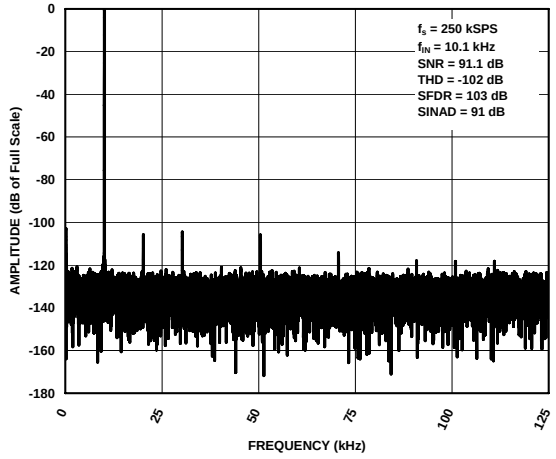

Figure 7. 10kHz FFT, VREF = 5V

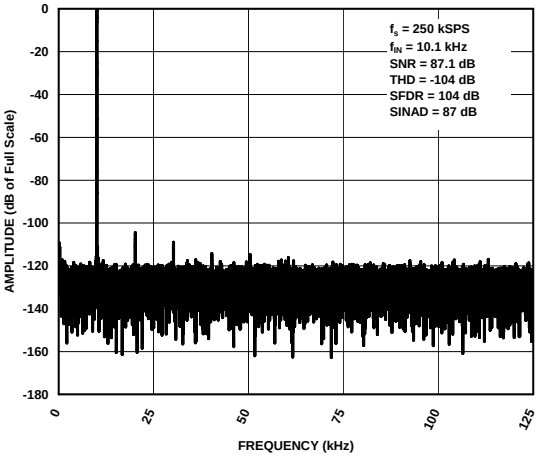

Figure 10. 10kHz FFT, VREF = 2.5V

TERMINOLOGY

Least Significant Bit (LSB)
The LSB is the smallest increment that can be represented by a converter. For an analog-to-digital converter with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\mathrm{V}) = \frac{V_{REF}}{2^N}$$

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (38.14µV). The unipolar offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full-scale. The gain error is the deviation in LSB (or % of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or % of full-scale range), which includes the effects of the offset error.

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Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{\mathrm{dB}} - 1.76)/6.02$$

and is expressed in bits.

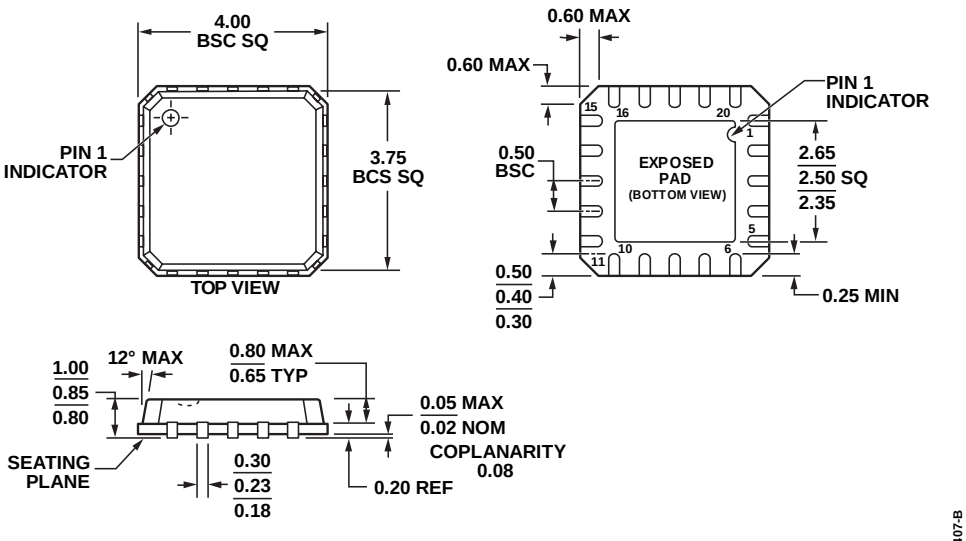
Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a DC to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel and is expressed in dB.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\mathrm{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\mathrm{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}(Min)$ = minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}(25°C)$ = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 11. 20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
4 mm × 4 mm Body, Very Thin Quad
(CP-20-4)
Dimensions shown in millimeters

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ORDERING GUIDE

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